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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/054,601	01/22/2002	Leonard Forbes	303.504US3	8301

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EXAMINER	
SANTIAGO, MARICELI	

ART UNIT	PAPER NUMBER
2879	

DATE MAILED: 01/31/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/054,601	FORBES ET AL.	
	Examiner	Art Unit	
	Mariceli Santiago	2879	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-31 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-31 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 22 January 2002 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Objections

Claim 28 is objected to because of the following informalities:

Claim 28 recites the limitation "forming a polysilicon cone includes forming a metal silicide on the polysilicon cone", the recitation objectionable since the preceding base claim refers to "a number of polysilicon cones". Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 19 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 19 recites the limitation "the porous oxide layer" in line 1. There is insufficient antecedent basis for this limitation in the claim.

Claim 19 recites the limitation "a gate", this limitation renders the claim indefinite, since where a claim directed to a device can be read to include the same element twice, it is considered indefinite. *Ex parte Kristensen*, 10 USPQ2d 1701 (Bd. Pat. App. & Inter. 1989).

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1-15 and 26-28 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 32-37, 39-43 and 45-48 of U.S. Patent No. 6,232,705 B1. Although the conflicting claims are not identical, they are not patentably distinct from each other because of the following reasons.

Application SN 10/054,601	U.S. Patent No. 6,232,705	Reasons for rejection under obviousness double patenting
Claim 1	Claim 32	Same subject mater. Patent '705 claims a method of forming a field emitter device on a substrate, comprising forming a polysilicon cone on the substrate, forming a porous oxide layer on the substrate, wherein the porous oxide layer and the polysilicon cone are formed from a single layer of polysilicon, forming a gate layer on the porous oxide layer, isolating the polysilicon cone form the gate, and forming an anode opposing the polysilicon cone.
Claim 2	Claim 33	Same subject matter. Patent '705 claims a method wherein forming the field emitter device on a substrate includes forming the device on a silicon dioxide (SiO_2) substrate.
Claim 3	Claim 34	Same subject matter. Patent '705 claims a method wherein forming the polysilicon cone and the porous oxide layer from a single layer of polysilicon includes masking a cathode region on the substrate.
Claim 4	Claim 35	Same subject matter. Patent '705 claims a method wherein masking the cathode region includes forming an oxide-nitride-oxide (ONO) mask over the cathode region, forming the porous oxide layer, removing the top oxide from the ONO mask, etching the nitride to reduce the width of the mask, and forming the gate layer on the porous oxide and the mask.
Claim 5	Claim 36	Same subject matter. Patent '705 claims a method wherein masking the cathode region includes forming an oxide layer over

		the cathode region, forming a first nitride layer over the oxide layer in order to form a structure which reflects the final pattern of the gate layer, forming a second nitride layer over the first nitride layer and the single polysilicon layer, etching the second nitride layer, leaving the second nitride layer only on the sidewalls of the structure, and forming the porous oxide layer, removing the first and second nitride layers, and forming the gate layer on the porous oxide and the oxide layer.
Claim 6	Claim 37	Same subject matter. Patent '705 claims a method wherein forming the porous oxide layer include performing an anodic etch on the single polysilicon layer in an insulator region of the substrate to form porous polysilicon, and oxidizing the porous polysilicon.
Claim 7	Claim 39	Same subject matter. Patent '705 claims a method wherein forming a polysilicon cone includes forming a metal silicide on the polysilicon cone.
Claim 8	Claim 40	Same subject matter. Patent '705 claims a method wherein forming a metal silicide on the polysilicon cone includes using an electron beam to deposit molybdenum (Mo) on the polysilicon cone.
Claim 9	Claim 41	Same subject matter. Patent '705 claims a method wherein forming a gate on the porous oxide layer includes forming a refractory metal gate.
Claim 10	Claim 42	Same subject matter. Patent '705 claims a method wherein isolating the polysilicon cone from the gate includes shaping the gate material in close proximity to a top surface of the polysilicon cone using a lift-off technique, and removing the porous oxide layer adjacent to the polysilicon cone.
Claim 11	Claim 48	Same subject matter. Patent '705 claims a method wherein forming the porous oxide layer includes performing an anodic etch on the single polysilicon layer in an insulator region of the substrate to form porous polysilicon, and oxidizing the porous polysilicon.
Claim 12	Claim 43	Same subject mater. Patent '705 claims a field emitter device on a substrate, comprising a cathode formed in a cathode region of the substrate, a gate insulator formed in an insulator region of the substrate, a gate formed on the gate insulator, and an anode opposing the cathode, the field emitter device formed by a method

		comprising forming a polysilicon cone on the substrate, forming a porous oxide layer on the substrate, wherein the porous oxide layer and the polysilicon cone are formed from a single layer of polysilicon, forming a gate layer on the porous oxide layer, isolating the polysilicon cone form the gate, and forming an anode opposing the polysilicon cone.
Claim 13	Claim 45	Same subject matter. Patent '705 claims a field emitter wherein forming the polysilicon cone and the porous oxide layer from a single layer of polysilicon includes masking a cathode region on the substrate.
Claim 14	Claim 46	Same subject matter. Patent '705 claims a field emitter wherein masking the cathode region includes forming an oxide-nitride-oxide (ONO) mask over the cathode region, forming the porous oxide layer, removing the top oxide from the ONO mask, etching the nitride to reduce the width of the mask, and forming the gate layer on the porous oxide and the mask.
Claim 15	Claim 47	Same subject matter. Patent '705 claims a field emitter wherein masking the cathode region includes forming an oxide layer over the cathode region, forming a first nitride layer over the oxide layer in order to form a structure which reflects the final pattern of the gate layer, forming a second nitride layer over the first nitride layer and the single polysilicon layer, etching the second nitride layer, leaving the second nitride layer only on the sidewalls of the structure, and forming the porous oxide layer, removing the first and second nitride layers, and forming the gate layer on the porous oxide and the oxide layer.
Claim 26	Claim 32	Claim 26 is rejected for the same reasons stated in the rejection of claim 1 above. Furthermore, while Patent '705 claims a polysilicon cone, mere duplication of the essential working parts of a device involves only routine skill in the art. Thus, it would have been obvious to one having ordinary skill in the art at the time the invention was made to form multiple polysilicon cones and anodes, since mere duplication of essential parts of the invention is considered within the skill of the art. *In re Harza*, 274 F. 2d 669,124 USPQ 378 (CCPA 1960).

Claim 27	Claim 37	Claim 27 is rejected for the same reasons stated in the rejection of claim 6 above.
Claim 28	Claim 39	Claim 28 is rejected for the same reasons stated in the rejection of claim 7 above.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 3, 9, 10-13, 16, 19, 20, 22, 26 and 27 are rejected under 35 U.S.C. 102(b) as being anticipated by Lee (US 5,458,518).

Regarding claim 1, Lee discloses a method for forming a field emitter device on a substrate (see Embodiment 1, Column 3, lines 44-67), comprising forming a polysilicon cone (21) on the substrate (10), forming a porous oxide layer (24) on the substrate (10), wherein the porous oxide layer (24) and the polysilicon cone (21) are formed from a single layer of polysilicon, forming a gate layer (22) on the porous oxide layer (24), isolating the polysilicon cone from the gate (22), and forming an anode (3) opposing the polysilicon cone (21).

Regarding claim 3, Lee discloses a method wherein forming the polysilicon cone and the porous oxide layer from a single layer of polysilicon includes masking (11) a cathode region (21) on the substrate.

Regarding claim 9, Lee discloses a method wherein forming a gate on the porous oxide layer includes forming a refractory metal gate (Column 4, lines 9-16).

Regarding claim 10, Lee discloses a method wherein isolating the polysilicon cone from the gate includes, shaping the gate material in close proximity to a top surface of the polysilicon

cone using a lift-off technique, and removing the porous oxide layer adjacent to the polysilicon cone (Column 4, lines 9-16).

Regarding claim 11, Lee discloses a method wherein forming the porous oxide layer includes performing an anodic etch on the single polysilicon layer in an insulator region of the substrate to form porous polysilicon and oxidizing the porous polysilicon (Column 3, lines 46-66).

Regarding claim 12, Lee discloses a method for forming a field emitter device on a substrate (10), comprising a cathode (21) formed in a cathode region of the substrate, a gate insulator (24) formed in an insulator region of the substrate, a gate (22) formed on the gate insulator, and an anode (3) opposing the cathode, the field emitter device formed by a method (see Embodiment 1, Column 3, lines 44-67) comprising forming a polysilicon cone (21) on the substrate (10), forming a porous oxide layer (24) on the substrate (10), wherein the porous oxide layer (24) and the polysilicon cone (21) are formed from a single layer of polysilicon, forming a gate layer (22) on the porous oxide layer (24), isolating the polysilicon cone from the gate (22), and forming an anode (3) opposing the polysilicon cone (21).

Regarding claim 13, Lee discloses a field emitter wherein forming the polysilicon cone and the porous oxide layer from a single layer of polysilicon includes masking (11) a cathode region (21) on the substrate.

Regarding claim 16, Lee discloses a method (see Embodiment 1, Column 3, lines 44-67) for forming a field emitter device on a substrate (10), comprising forming a cathode (21) on the substrate, forming a gate insulator layer (24) on the substrate (10), wherein the gate insulator layer and the cathode are formed from a single layer of polysilicon, forming a gate layer (22) on the gate insulator layer, isolating the cathode from the gate and forming an anode (3) opposing the cathode (21).

Regarding claim 19, Lee discloses a method wherein the forming a gate on the porous oxide layer includes forming a refractory metal gate (Column 4, lines 9-16).

Regarding claim 20, Lee discloses a method (see Embodiment 1, Column 3, lines 44-67) for forming a field emitter device on a substrate (10), comprising forming a number of cathodes (21) on the substrate, forming a gate insulator layer (24) on the substrate (10), wherein the gate insulator layer and the number of cathodes are formed from a single layer of polysilicon, forming a gate layer (22) on the gate insulator layer, isolating the number of cathodes from the gate and forming a number of anodes (3) opposing the number of cathode (21).

Regarding claim 22, Lee discloses a method wherein forming the gate insulator layer includes forming a porous oxide layer (24).

Regarding claim 26, Lee discloses a method for forming a field emitter array on a substrate (see Embodiment 1, Column 3, lines 44-67), comprising forming a number of polysilicon cones (21) on the substrate (10), forming a porous oxide layer (24) on the substrate (10), wherein the porous oxide layer (24) and the number of polysilicon cones (21) are formed from a single layer of polysilicon, forming a gate layer (22) on the porous oxide layer (24), isolating the number of polysilicon cones from the gate (22), and forming a number of anodes (3) opposing the number of polysilicon cones (21).

Regarding claim 27, Lee discloses a method wherein forming the porous oxide layer (24) includes performing an anodic etch on the single polysilicon layer in an insulator region of the substrate (10) to form porous polysilicon (12), and oxidizing the porous polysilicon (Column 3, lines 46-65).

Claim Rejecti ns - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2, 17, 21 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee (US 5,458,518).

Regarding claim 2, 17, 21 and 24, Lee discloses the claimed invention except for the limitation of forming the device on a silicon dioxide (SiO_2) substrate. It has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin*, 125 USPQ 416. Thus, it would have been obvious to one having ordinary skills in the art at the time the invention was made provide a silicon dioxide (SiO_2) substrate, since the selection of known materials for a known purpose is within the skill of the art.

Claims 7, 8, 18 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee (US 5,458,518) in view of Lee (US 5,401,676).

Regarding claims 7, 8, 18 and 28, Lee ('518) discloses the claimed invention except for the limitation of forming a polysilicon cone includes forming a metal silicide on the polysilicon cone, the metal silicide made by depositing molybdenum (Mo) on the polysilicon cone. However, in the same field of endeavor, Lee ('676) discloses a method for forming a field emitter device wherein forming a polysilicon cone (37) includes forming a metal silicide (40) on the polysilicon cone, the metal silicide made by depositing molybdenum (Mo) on the polysilicon cone. The metal silicide efficiently strengths the emission characteristic of the emitter, and an

emitter is made which can block the permeation of the metal component to the insulating layer (Column 4, lines 18-28). Thus, it would have been obvious at the time the invention was made to a person having ordinary skills in the art to incorporate the metal silicide made by depositing molybdenum (Mo) on the polysilicon cone in order to efficiently strengthen the emission characteristic of the emitter, and provide an emitter which can block the permeation of the metal component to the insulating layer.

Claims 23, 25 and 29-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee (US 5,458,518) in view of Zimlich et al. (US 5,910,791).

Regarding claim 23, Lee discloses a method (see Embodiment 1, Column 3, lines 44-67) for forming a field emitter device on a substrate (10), comprising forming a number of cathodes (21) on the substrate, forming a gate insulator layer (24) on the substrate (10), wherein the gate insulator layer and the number of cathodes are formed from a single layer of polysilicon, forming a gate layer (22) on the gate insulator layer, isolating the number of cathodes from the gate and forming a number of anodes (3) opposing the number of cathode (21). Lee is silent in regards to the limitation of coupling a row decoder and a column decoder to the field emitter array, and coupling a processor to the row and column decoders. However, in the same field of endeavor, Zimlich discloses a field emitter device comprising a row decoder and a column decoder coupled to the field emitter array, and further coupling a processor to the row and column decoders in order to operate the device, since it is well known in the art to provide such elements for general driving of the display. Thus, it would have been obvious at the time the invention was made to a person having ordinary skills in the art to incorporate a row decoder and a column decoder coupled to the field emitter array, and further coupling a processor to the

row and column decoders in order to operate the device, since it is well known in the art to provide such elements for general driving of the display.

Regarding claim 25, Lee discloses a method wherein forming a number of cathodes on the substrate includes forming a number of polysilicon cones (21) on the substrate (10).

Regarding claim 29, Lee discloses a method for forming a field emitter array on a substrate (see Embodiment 1, Column 3, lines 44-67), comprising forming a number of polysilicon cones (21) on the substrate (10), forming a porous oxide layer (24) on the substrate (10), wherein the porous oxide layer (24) and the number of polysilicon cones (21) are formed from a single layer of polysilicon, forming a gate layer (22) on the porous oxide layer (24), isolating the number of polysilicon cones from the gate (22), and forming a number of anodes (3) opposing the number of polysilicon cones (21). Lee is silent in regards to the limitation of coupling a row decoder and a column decoder to the field emitter array, and coupling a processor to the row and column decoders. However, in the same field of endeavor, Zimlich discloses a field emitter device comprising a row decoder and a column decoder coupled to the field emitter array, and further coupling a processor to the row and column decoders in order to operate the device, since it is well known in the art to provide such elements for general driving of the display. Thus, it would have been obvious at the time the invention was made to a person having ordinary skills in the art to incorporate a row decoder and a column decoder coupled to the field emitter array, and further coupling a processor to the row and column decoders in order to operate the device, since it is well known in the art to provide such elements for general driving of the display.

Regarding claim 30, Lee discloses a method wherein forming the porous oxide layer (24) includes performing an anodic etch on the single polysilicon layer in an insulator region of the

substrate (10) to form porous polysilicon (12), and oxidizing the porous polysilicon (Column 3, lines 46-65).

Regarding claim 31, Lee discloses a method wherein the forming a gate on the porous oxide layer includes forming a refractory metal gate (Column 4, lines 9-16).

Other Prior Art Cited

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Das et al., in US 5,627,427, discloses a silicon tip field emission cathode and method of manufacturing the same.

Laou et al., in US 5,857,885, discloses a method of forming field emission devices with self-aligned gate structure.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mariceli Santiago whose telephone number is (703) 305-1083. The examiner can normally be reached on Monday-Friday from 7:00 AM to 3:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nimesh Patel, can be reached on (703) 305-4794. The fax phone number for the organization where this application or proceeding is assigned is (703) 308-7382. Additionally, the following fax phone numbers can be used during the prosecution of this application (703) 872-9318 (for response before a Final Action) and (703) 872-9319 (for response after a Final Action).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

1/24/03

Mariceli Santiago
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Kenneth J. Ramsey
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